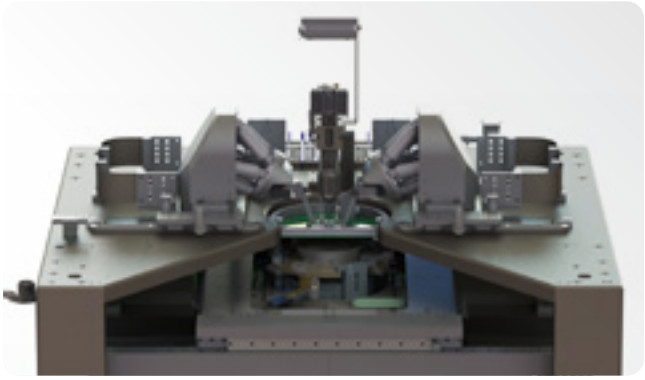
SIRIUS Photonic Test Prober

IMS

TAKING YOU
STEPS AHEAD

SIRIUS
Photonic Test Prober



Testing Photonic Integrated Circuits before packaging is crucial. Up to 80% of the costs related to PIC development are associated with packaging and testing.

Packaging defective dies wastes both valuable time and money. SIRIUS, our Photonics Testing Prober, is designed to take care of this problem. With Simultaneous electrical and optical ports connection, testing PICs became easier than ever. SIRIUS is an advanced wafer-level PIC functional tester that identifies Known Good Dies (KGDs) for further back-end processes. With user-friendly inputs and a detailed wafer map, it is easier to select the perfect dies that are ready for the next stage.

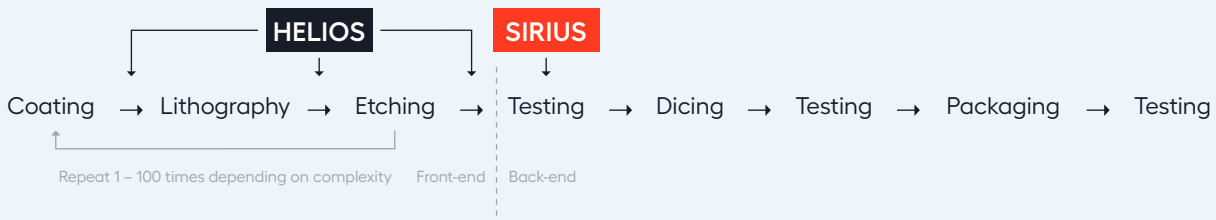
SIRIUS scales seamlessly with your advanced and new technology, whether you are running low-volume high-mix or high-volume low-mix production. We made sure to support all of your testing needs with extensive and modular PXIe format instrumentation.

Fully adaptable to your needs

The most standout feature of the Photonics Testing Prober is its remarkable adaptability. It seamlessly performs tests on various material platforms and electro-optic I/O configurations. Our novel electrical and optical probe exchange systems lets you change probes within 30 minutes. This allows users to spend time on the tasks that matter.

With state of the art micro manipulators, our system achieves reproducible low-loss alignment to PIC optical I/O ports. The system connects to your MES using the SECS/GEM interface and it is compatible with SEMI E122/E30 standards.

Where are our machines used?



System specifications
Photonic Test Prober

Cleanroom requirements	
Environment	ISO 9 or better
Floor vibration	VC-C or better (standard cleanroom)
Machine footprint	1.8 m x 1.9 m (excluding 1 m free space around)
Network	1XRJ45 connection, CAT 5e
Electrical interface	400 VAC, 32A connection, Max fuse 25A
Gas, air or vacuum	> 6 bar pneumatic connection
Cable feed through	Bottom or top of the machine

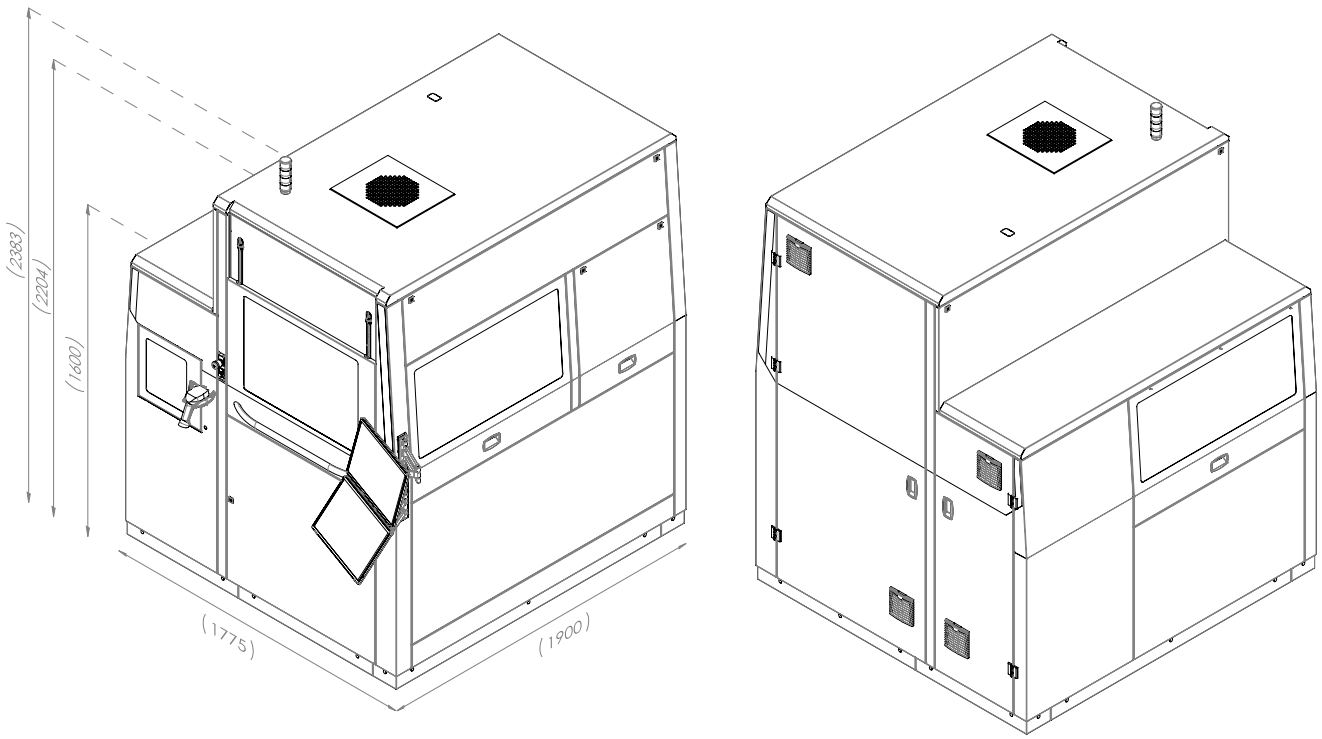
Hardware system specifications	
Wafer table compatible	4 inch to 8 inch wafers
Wafer loading	Automatic using Cassettes or SMIF pods
Wafer chuck	Thermally conditioned up to +50 °C
Dynamic stability	Up to 100 nm
Simultaneous electro-optical probing	DC probing + Surface coupling (0 to 10 degrees)
Multi-channel DC probing	9" IC electrical probe card up to 3000 pads
Multi-channel optical probing	2x 16 channels
Instrument rack	Fully customized PXIe format, Visible, O- and C-Band
Test Cell Controller	Test runner to run and handle test protocols (recipes)
Result viewer	DPlus, EZ-SubstrateMap
Typical instruments	Optical spectrum analyzer, Digital Power Supply, Power meter, Laser source, broadband source for alignment, Optical switches
Automated calibration procedure	Fiducials for probe card needles, optical probes and wafer chuck, Customer specific alignment wafer markers

Data handling specifications	
Interface protocol	SEC/GEM interfacing with MES according to SEMI E30 With specific additions for the test equipment described in SEMI E122
Data management	Exchange test protocols, wafer maps, recipes and test reports in EZ-MES

System specifications
Photonic Test Prober

Optical coupling specifications	
Coarse alignment accuracy	± 1 µm (Tx, Ty, Tz) and ± 1 degrees (Rx, Ry, Rz)
Fine alignment accuracy	± 10 nm t_x; ± 20 nm t_y; ± 10 nm t_z
Resolution	0.3 nm x,y,z
Alignment mode	Continuous alignment
Alignment time	< 1 s
Stable wafer chuck	XY accuracies, Acceleration 20 m/s^2 Accuracy < 1 µm Jitter < 100 nm

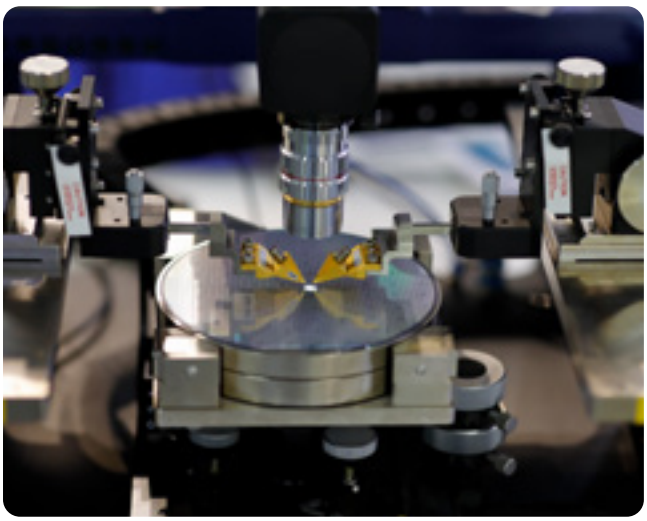
Dimensions of SIRIUS for your production floor



Everything you need to know
Photonic Test Prober

Automated electro-optical testing of PICs gives you the advantages of reducing production costs and faster chip design iterations. SIRIUS helps and empowers users to perform trial-and-error on their chip designs. With complete stack data of wafers, SIRIUS empowers application developers to perform quick design iterations of their chip. This data can be used to further improve products or even a foundry's PDK.

As the probe exchange system is easily interchangeable, various chip I/O configurations can be tested. Our system stands out in its ability to automatically calibrate incoming probe card layouts and adjust the recipe on the run.



KEY BENEFIT

Identify Known Good Dies

Identify your Known Good Dies (KGD) early in the process. This makes it easier to save costs in the back-end of line.

KEY BENEFIT

Fast changeover time

With a changeover time of less than 30 minutes it is quick and easy to interchange the probe cards. Therefore making SIRIUS ideal for High-Mix Low-Volume configurations.

KEY BENEFIT

High Precision Alignment

Thanks to the 6-DOF optical alignments and a high stand still stability, the system can align precisely to the optical I/O ports and achieves low-losses.

KEY BENEFIT

Unique Architecture

Modular design allows adaptation, reconfiguration and re-tooling to a wide range of (future) products.

Experience the power of SIRIUS

Are you ready to take full control of wafer probing? Our system is ready to test your samples. Get in touch with us through **sales@ims-nl.com** or **+31 546 805 580** and we will help you out.